University of Oklahoma
School of Electrical and Computer Engineering
ECE 5833/4833: VLSI Digital System Design
Fall 2024

Time: Monday 9:00 AM - 11:40 AM

Place: Carson Engr Ctr (CEC) 205/206

Instructor: Mike Banad, bana@ou.edu

Class TA: Reza Ahmadvand, iamrezaahmadvand@ou.edu

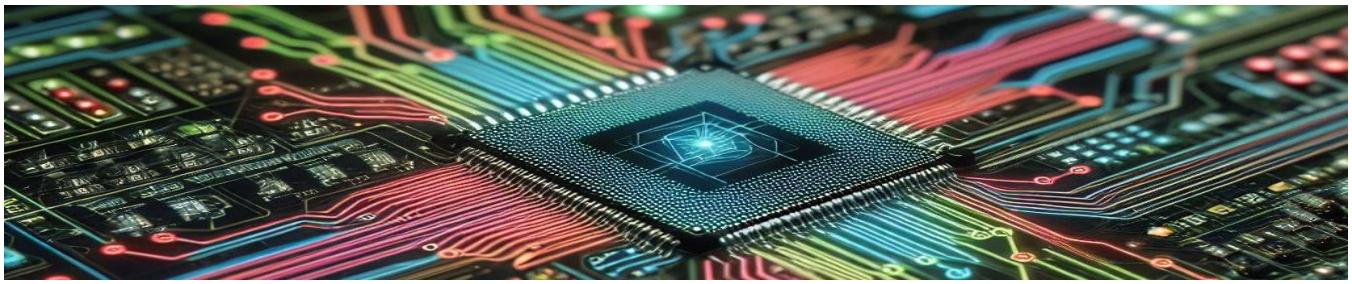
Office Hours: Tuesday, from 8:30 - 10:00 AM, in DEV 342, and other times by appointment. TA office hours are Wednesday, 1:00 PM – 3:00 PM in CLC 205/206 (Classroom). Note: Office hours are times in which you may ask questions about course content, delve deeper into the topic through conversation with me, share concerns you have about the course, and/or explore career or graduate school and job opportunities with me in this field. The office hours not only help you but also help me to know the questions my students have so that I may adjust my teaching approach as needed.

Learning Management System/website: Canvas Course page (https://canvas.ou.edu/)

Course Prerequisites: ECE 2214. Digital Design, ECE 3873 (Electrical and Computer Engineering Electronics Laboratory), and ECE 3723. Electrical Circuits II, or permission of the instructor.

Course Description: This course introduces Very-Large-Scale Integrated (VLSI) systems design methods; complementary Metal-Oxide Semiconductor (CMOS) technology is emphasized. VLSI Computer-Aided Design (CAD) tools and CMOS layout rules and techniques. This course covers not only the layout and the design of digital logic in VLSI/CMOS technology, but also the beyond-CMOS technology roadmap based on emerging materials and architecture. Project-oriented. No student may earn credit for both 4833 and 5833.

What is VLSI Design? VLSI design deals with designing integrated circuits (ICs) that contain a very large number of transistors and other electronic components on a single chip. These chips can contain millions or even billions of transistors. VLSI design involves the integration of complex digital and analog circuits onto a single semiconductor substrate. VLSI design encompasses not only the design of individual circuits but also the design and layout of the entire chip, including the interconnections between various components. It involves high-level architectural design, logic design, physical design, and verification at different levels of abstraction.



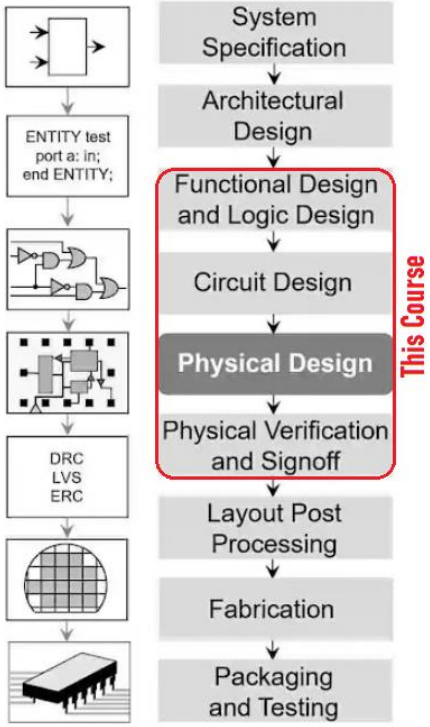
Course Goals: (1) Identify the various IC fabrication methods; (2) Express the Layout of simple CMOS circuits; (3) Apply the Lambda-based design rules to implement the physical layout for subsystem integrated circuits; (4) Be aware of beyond-CMOS technology.

Learning Outcomes:

1. Understand the basic physics and modeling of MOSFETs to design VLSI circuits.
2. Learn the basics of fabrication and layout of CMOS integrated circuits.
3. Apply CMOS technology-specific layout rules in the placement and routing of transistors and interconnect, and verify the functionality, timing, power, and parasitic effects.
4. Employ the characteristics of CMOS devices to construct static and dynamic CMOS Logic operational devices using state-of-the-art CMOS technologies and processes.
5. Design and evaluate a significant VLSI design project having a set of objective criteria and design constraints.
6. Learn about the possible beyond-CMOS technology such as neural-inspired circuits.

Texts and Materials:

This course will use materials from multiple open-access sources, including the main textbook below, which is available through the University of Oklahoma Libraries. The PowerPoint slides of lectures and any other information will be available through the canvas platform. To complete your VLSI design projects, you may need to review literature, available to the general public via the internet, to come up with the circuit architecture. Reviewing peer-reviewed articles is encouraged in this course to provide you with a solid foundation for our class discussions and project design activities. As Tanner L-Edit (MentorGraphic: Simense EDA Software) will be used as a layout design platform for your project designs, the third reference book below can be used as your reference book for this software. Lab instructions and handouts will be given during laboratory hours as needed. Mentor Graphics Education Center provides a series of Instructions on YouTube (https://www.youtube.com/watch?v=iyFfpjcS8dE).



A. Text Book:

1. Jan M. Rabaey, Anantha Chandrakasan, and Borivoje Nikolic, Digital Integrated Circuits, Prentice Hall/Pearson, 2003, 2nd edition.
2. Powerpoint slides and online resources.

B. Reference Books:

1. Neil Weste and David Harris, CMOS VLSI Design – A Circuits and Systems Perspective, Pearson/Addison-Wesley, 2011, 4th edition.
2. R. Jacob Baker, CMOS – Circuit Design, Layout, and Simulation, IEEE/Wiley Inter -Science, Revised 2nd Edition, 2008.
3. John P. Uyemura, Physical Design of CMOS Integrated Circuits Using L-Edit 1st Edition, PWS Publishing Company, 1995.

About Your Instructor:

My educational training has taken me to various positions in industry and academia related to emerging electronic devices and circuit design. Notably, I initially enrolled in this course as a student over a decade ago, and my passion for the subject has led me to subsequently teach it at several other universities. The current course provides a foundation for CMOS technology, which is the result of more than 60 years of R&D, with a market size of $550 billion in 2022. At OU, I am teaching this course and a new course based on my research interest in beyond-CMOS technology. I am also establishing a new lab “Neuromorphic Intelligent Computing Systems.” The mission of this lab is described by the US Nanotechnology-Inspired Grand Challenge for Future Computing: "Create a new type of computer that can proactively interpret and learn from data, solve unfamiliar problems using what it has learned, and operate with the energy efficiency of the human brain." So, you may ask how this can relate to VLSI design. Well, the current VLSI technology is based on digital CMOS technology that works in von Neumann architecture (separate computing and memory units). The term “Beyond CMOS” refers to potential future technologies that expand beyond the present CMOS scaling limits by overcoming and resolving many problems in CMOS technology such as dramatic heating effects at the nanoscale, or what so-called memory wall and power wall because of von Neumann architecture. My research aims to design energy-efficient and high-speed computing-in-memory (CIM) circuits by inspiring the electrical activities of neurons and synapses and neural networks in the brain. This approach can overcome the inherent challenges of current computing systems (memory and power walls) designed with digital CMOS technology. NICS aims to combine new technological advances in nanomaterials, new devices and circuits, and computer systems and architectures to bring AI on chips with very low power consumption and processing latency. I am enthusiastic about my field and look forward to answering questions and engaging with each of you. If you are interested to know more about my research or would like to join my research group to get research experience or pursue graduate study, please don’t hesitate to deliver your interest and ideas. Every semester, I learn from my students, which keeps me passionate about teaching and research.

Teaching Philosophy:

My goal is to create a class in which everyone is welcome, included, and able to learn and succeed. Because we all learn in different ways, the topics are discussed by incorporating lectures, projects, homework, and circuit design ideas from peer-reviewed academic articles. I believe strongly in our capacity to learn when given the appropriate support and resources. We are always learning to get more knowledge in life, while learning new subjects can cause discomfort. Remember, the more we learn, the less we know. It might be confusing to connect meaningful relations between the topics. Learning is a process. You need to be patient while focusing on completing the class assignments and projects to learn by doing the circuit designs in your projects. I am here to affirm that it is okay that you don’t know everything already, and that’s why you are here: to learn. I hope to foster a collaborative learning environment, especially in your circuit design projects, where you can support one another in your academic growth.

Expectations:

What you can expect from me:

- Timely commencement and conclusion of classes.
- Homework and assignments that comprehensively cover course material and align with the learning objectives, respecting the time commitment appropriate for a 3-credit course.
- Response to emails within 48 hours on weekdays and 72 hours during weekends.
- Maintain office hours, with advance notice of any changes.
- Ample opportunities for you to demonstrate and receive feedback on your learning, aiding your progress and self-assessment.
- Examinations that reflect class content and assigned homework are challenging yet manageable, with our low-risk assignments aimed at building your confidence and competence.
- Project work that encourages further reading and understanding of circuit and layout designs from academic literature, fostering diverse approaches and self-directed learning in your design work.

What you cannot expect from me:

- Extensions on assignments. Everyone is allotted the same time frame for completion. No personalized request is accepted except with a legitimate excuse letter.
- Extra material or information for exams beyond what is shared with the entire class as it jeopardizes the fairness of grades.
- Complete responses to incomplete or late inquiries about assignments or projects.
- Resolution of access issues to class software. These are beyond my control and IT is responsible for the computers and softwares; time management is crucial for meeting project deadlines.
- Responsibility for lost project files. Ensure you back up your work on a personal memory drive to avoid losing points or grades.

What I expect from you:

- Academic Integrity: Familiarize yourself with the university's academic integrity guidelines at http://www.ou.edu/provost/pronew/content/integritymenu.html. Integrity and honesty are paramount in our academic community. Any form of dishonesty is a serious offense and may lead to severe consequences, including suspension.
- Maintenance of a learning-conducive classroom environment: Arrive on time, avoid unnecessary exits and re-entries, and respect everyone's right to a distraction-free learning space.
- Active engagement in class: Participate, share your understanding, and seek clarification when needed. Engaging with both the theoretical and practical aspects of the course is key to your learning.
- Regular note-taking: This is especially helpful since the class meets once a week, and details, such as software operation, might slip your memory.
- Consistent effort on homework and projects: Spend sufficient time each week understanding and working on problems and layout designs. Seeking help when needed ensures you have the necessary resources to be actively involved in the learning process.

Learning Activities, Assignments, and Assessments:

This course will engage you with various activities and assignments to learn VLSI design. You will read textbooks and online resources before class and actively participate in learning activities in class to help deepen your understanding of the content. You will collaborate with a small group on several collaborative projects to develop the layout and test the layout design of several VLSI circuits. There will be several collaborative projects such as the development of flip flops, shift registers, counters, oscillators, etc. These project-based activities can deepen your critical thinking, demonstrate your mastery of the topics, and develops collaboration skills, which is highly valued by employers. A considerable portion of this class will be spent working on the projects, including readings and exploring different experiences, ideas, and perspectives for your VLSI projects. We also expect you to participate in the activities and discussions that take place in class throughout the semester and work together as a team to support each other's learning. You will work in a small group, likely 2 members, to work with your peers to develop these projects. Using design rules and criteria, you will receive feedback from your instructor and peers about your project. You will be given a precise template to write the report of your project. A general description of each project will be distributed in class while many details to complete your project depend on your choices. You must provide enough information about your approach and methodology in your report. Projects' reports are due two weeks before the end of the semester. The last two weeks are dedicated to your presentations. It is important to meet the deadlines for any learning activities, projects, and assignments. The quality of all written assignments and presentations will be evaluated using a rubric.

Assigning Grades:

The final grade you receive at the end of the course will be determined by the accumulated points you earn on individual assignments, midterm and final exams, and your contribution to your project. The number of points you earn is based on the quality of the work you submit. The lowest homework grade will be dropped and will not be counted toward your final grade. I will evaluate your participation, team performance, and efforts based on your reports and presentations, as well as engagement and contributions in group activities of your design projects. The design project will be implemented during laboratory hours. Every group will be required to classroom presentation of the project. The report is due two weeks before your final exam. The laboratory is an integral part of the course and will be the second part of the course after the lecture. Homework and project will require extensive use of L-EDIT, CEDAR Logic Simulator (or equivalent available Logic Simulator), and SPICE circuit simulators.

Your VLSI Term Project:

For your project, you have the freedom to choose from a selection of typical logic modules, including but not limited to Voltage Controlled Oscillators, Digital Controlled Oscillators, 4-bit Shift Registers, 4-to-1 Multiplexers, Full Adder, Counters, 4-bit Comparators, and Arithmetic Logic Units. Alternatively, you are encouraged to explore your own interests and choose a project that aligns with your personal passions and expertise. To facilitate your project selection, I am available for consultation. Please feel free to reach out to me to discuss your project ideas and share any reference materials or resources that may be relevant. Your project should be a reflection of your individual interests and aspirations in the realm of logic design.

The project report should be written either individually or jointly in the following format.

- Title and Project Description
- Full Logic Level Block Diagram
- Cell Level Description/Cell library
- Logic Level Diagrams, Logic-level Simulations, and Truth Tables
- Circuit/Transistor Level Diagram with Relevant Node Numbers
- L-Edit Layout of Cells
- SPICE Netlist Code and Simulation Results
- Plots of Cell Libraries &
- Layout of Complete VLSI Design
- Screenshot of Design Rule Check (DRC)
- References

The project report must be word-processed (or PDF) and submitted in its original format (preferably as a soft copy), accompanied by your PowerPoint presentation slides and simulation files, all consolidated into a single ZIP file.

The rubrics for your project include:

Table 1		
Rubric		**Point**
Proposal Presentation	Clearly explain your reference, including the circuit schematic and its functionality (Informative Slides should be submitted a week before the presentation date)	10 points
Report: Project Description	Clearly stated project title and Comprehensive project description that outlines the objectives and goals	5 points
Full Logic Level Block Diagrams	Detailed and well-labeled logic-level block diagram of the VLSI design, or Equivalent logic Schematics	10 points
Cell Level Description/Cell Library	A thorough description of the cell library, including cell functionality and characteristics. Explanation of how cell library components are assessed in testbed design, and how the cell contributes to the project.	10 points
Logic Level Diagrams, Logic-level Simulations, and Truth Tables	Clear logic-level diagrams with proper annotations. Simulations demonstrating the logical behavior. Truth tables for critical components, if applicable.	10 points
Transistor Level Diagram	Detailed circuit/transistor level diagrams with labeled nodes. Explain any testbed design used to assess the operation of the circuit design.	10 points
L-Edit Layout of Cells	Presentation of L-Edit layouts for each cell. Explanation of any design considerations or constraints	10 points
SPICE Netlist Code and Simulation Results	SPICE codes and/or circuit schematics. Simulation results were included and discussed, showcasing	10 points

	the design's performance and functionality, which were described in previous sections.	
Layout of Complete VLSI Design	Layout of the entire VLSI design, showing interconnections and component placement.	10 points
Proof of Design Rule Check (DRC) with no error	Screenshot demonstrating that the design adheres to design rule constraints	5 points
Overall Organization and Clarity in Report	Logical flow and organization of the report. Clarity of presented subject and presentation of information	5 points
Overall Organization and Clarity in Presentation		5 points
		100 points

The instructions in Table 1 serve as general guidelines, and some sections may not apply to your project. For instance, your Cell-Level (Module-Level) Description might be identical to the Logic-Level (Gate-Level) Diagram if your complete design consists solely of gates without incorporating modules like flip-flops.

Grading Overview:

Table 2: Grading Overview, assignments total 100% and this table shows how they are weighted towards your final grade.

Assignment	**Percentage of Final Grade ECE 4833**	**Percentage of Final Grade ECE 5833**
Test I (will be scheduled with a week in advance notice)	10%	10%
Test II (will be scheduled with a week in advance notice)	10%	10%
Midterm Exam (9:30 AM-11:00 AM, Oct. 9, Mon)	20%	20%
Final Exam (9:30 AM - 11:00 AM, Dec. 4, Tue)	20%	20%
Homework Assignments/Pop Quizzes (will be assigned through the canvas with a week to submit them)	20%	10%
Lab Design Project (Report & Presentation, will be due two weeks before the final exam)	20%	30%*

***** The projects for ECE 5833 will take 50% more time to complete approximately.

Grading Scale: Your letter grade will be assigned based on the scale below.

A: 90-100%; B: 80-89.9%; C: 70-79.9%; D: 60-69.9%; F: 59.9% or below.

Table 3: Tentative Class Schedule (Subject to Change).		
Week/Date	**Topics, Readings, or Activities**	**Assignments and Exams Due**
08/19/2024	Syllabus Review, Introduction (Chapter 1)	Assign. HW1
08/26/2024	The Manufacturing Process & Design Methodology - IC Layout (Chapter 2), Introduction to Gate-level Logic Design software.	
09/09/2024	The Devices & Design Methodology (Chapter 3), Inverter design and simulation, Intro to Circuit Simulators (S-Edit, T-SPICE/H-SPICE),	Due HW1, Assign. HW2
09/16/2024	The Wire (Chapter 4): Capacitance, Resistance, and Inductance of VLSI Interconnects. More about Circuit Simulations in VLSI: Circuit designs with S-Edit platform	Due HW2,
09/23/2024	The CMOS Inverter (Chapter 5): Voltage Transfer Characteristics, Test I	Assign. HW3, **Test I**
09/30/2024	The CMOS Inverter (Chapter 5): Propagation Delay of an Inverter, Inverter sizing for propagation delay optimization, Intro to L-Edit Layout Design Environment	Due HW3.
10/07/2024		The Midterm Exam, Starts at 9:05 AM.
10/10/2024	Extra Office Hours have been posted.	**Last day to discuss the Project Plan and submit its slides.**
10/14/2024	The CMOS Inverter (Chapter 5): Inverter Sizing for Power Dissipation Optimization, Continue with Layout Design of an Inverter,	"**Project Plan Presentation**"
10/21/2024	The CMOS Inverter (Chapter 5): Power Dissipation: Dynamic, short circuit, and static components. Intro to Design Rule Check for Layout Design Environment	Assign. HW4, **Working on VLSI Term Project**
10/28/2024	Designing Combinational Logic Gates in CMOS Design Methodology (Chapter 6)	Due HW 4, **Working on the VLSI Term Project**
11/04/2024	Design Methodology – Complex Logic Gates Simulation, Different Layout Techniques for Complex Gates	Assign. HW5, **Working on VLSI Term Project**
11/11/2024	Designing Sequential Logic Circuits (Chapter 7)	Due HW 5, **Working on the VLSI Term Project**
11/18/2024	Design Methodology – Design Verification and Test of Manufactured Circuits, Characterizing Logic and Sequential Cells	Assign. HW6, **Test II**, **Working on the VLSI Term Project**
11/22/2024	Presentation Slides and Report Submission	
11/25/2024	Brief discussion about Beyond CMPS Technology, **Project Presentations**	Due HW 6, Project Report Due, "**Term Project Presentation"**
12/02/2024	Final Exam during the last lecture period *	Final Exam, 9:30-11:00 AM (CEC 205/206)
*Per Final Exam Policies: Classes meeting one day a week for more than one hour with a start time before 5:00 PM will have the final examination during the last lecture period. Classes in this format have been scheduled with sufficient meeting time during the semester to compensate for time lost in the final examination week.		

Course Policies:

I understand that many of us may be faced with unforeseen circumstances that can prevent us from completing our work on time or attending every session. Our late work and attendance policy exists, however, because your participation is crucial not only to your own success but also to contribute to the success of your peers who are able to learn from what you bring to the classroom.

Exam Policy: The tests, midterms, and final exams will be closed books and closed notes. Makeup exams will not be given. If you miss an exam and your absence is NOT officially excused, you will receive a zero grade for that exam. If you miss an exam and your absence is officially excused, your Final Exam grade (as a comprehensive exam) will be used in place of the missed exam grade. Unless otherwise stated, all exams will be comprehensive, covering the material from the entire course. Don't ask if the particular sections of the lecture will be in the exam. A one-page formula sheet will be available on the course website. It will be attached to the exam sheets to be used this sheet during the exam. Any equations or formulas not included on the provided sheet should be memorized beforehand. No answer about equations will be answered during exam.

Assignment Policy: Deadlines within this class have been created to allow for: peer engagement, for me to be able to assess if everyone is understanding the course material or if we need to revisit some of the subjects, and to provide me with the time needed to grade so that you can receive feedback as quickly as possible. So, late homework will not be accepted. Homework assignments will generally be due on Canvas at midnight on the published due date. The reason for this policy to not accept late assignments is that accepting a late assignment from one student is unfair to other students who may have stayed up all night to complete the assignment by the deadline. Another reason for this policy is that the overall learning outcomes of the assignment will not be achieved by delaying the posting of homework solutions. However, the due date might be extended a few days in some circumstances might be grated for all students. For paper and pencil homework assignments, you should scan or photograph your solution and upload it to Canvas.

Attendance Policy: In order to fully benefit from our class activities, you are expected to attend class and actively participate in the design project and lectures. Students are responsible for the content of the courses in which they are enrolled and lecture and laboratory attendance for this course are mandatory. Students have a responsibility to inform faculty prior to absences whenever possible. If you know that you are going to miss class because of an illness or an emergency, please email me to let me know. For this course, you have one automatically excused absence, which cannot be used on presentation days, exam reviews, or exam days. Any assignments that are due on the day would still need to be completed in accordance with our late work policy. Even on the day on which you use your automatically excused absence, you are expected to notify me. If I don't get an email from you and you are absent, I will assume that you have chosen not to attend. If you wait until the end of the semester to excuse your absences and share what happens that keeps you from attending, it would be late and we have to drop the course or apply for medical waivers. Additional excused absences are at my discretion (accommodations, as communicated, due to ADRC, medical emergencies, etc.). Again, if you miss class, it is your responsibility to find out from one of your colleagues what we covered and to get any information that I gave out in class.

Laboratory Policy: Not only is collaborative work during a design project an important professional skill to develop, it also helps you learn! Teaching one another and discussing the course content together during the design project will help you master the course objectives, as it will require you to develop a deeper understanding. But collaborative work must be truly

collaborative in order for everyone to reap the benefits. This means that you will have to contribute meaningfully and share labor. So, I expect everyone engages equally in the project during lab hours. The policy of the laboratory is the same as the lecture (described above). Eating and drinking are strictly forbidden in the laboratory. The use of cellphones is strictly prohibited and your engagement in the design project is essential.

Expectations for Academic Integrity and Plagiarism:
The overall goal of this course is your learning. In order to demonstrate that you have reached this goal, the work you turn in needs to be your own. If you work in a group, seek assistance from a tutor, or use one of the resources on campus, the work you turn in must be in your own words, demonstrating your own understanding of the material that you have gained through the learning process. Putting written work into your own words and citing your sources help you to avoid plagiarism. Penalties for serious offenses include a zero on the assignment and egregious offenses can even result in expulsion from the university, so it is important to understand expectations. The most serious offenses can often be avoided by citing sources—when in doubt, cite it! As part of our work together we will talk about how to accurately and responsibly cite sources, both to avoid plagiarism and strengthen your arguments. Plagiarism as defined by the OU Integrity Office includes (1) Copying words and presenting them as your own writing; (2) Copying words, even if you give the source unless you also indicate that the copied words are a direct quotation; (3) Copying words and then changing them a little, even if you give the source; and (4) Even if you express it in your own words, it is plagiarism to use someone else's idea as your own.

University Policies:

We also adhere to the following university policies in this course.

Mental Health Support Services

Support is available for any student experiencing mental health issues that are impacting their academic success. Students can either been seen at the University Counseling Center (UCC) located on the second floor of Goddard Health Center or receive 24/7/365 crisis support from a licensed mental health provider through TELUS Health. To schedule an appointment or receive more information about mental health resources at OU please call the UCC at 405-325-2911 or visit University Counseling Center. The UCC is located at 620 Elm Ave., Room 201, Norman, OK 73019.

Title IX Resources and Reporting Requirement

The University of Oklahoma faculty are committed to creating a safe learning environment for all members of our community, free from gender and sex-based discrimination, including sexual harassment, domestic and dating violence, sexual assault, and stalking, in accordance with Title IX. There are resources available to those impacted, including: speaking with someone confidentially about your options, medical attention, counseling, reporting, academic support, and safety plans. If you have (or someone you know has) experienced any form of sex or gender-based discrimination or violence and wish to speak with someone confidentially, please contact OU Advocates (available 24/7 at 405-615-0013) or University Counseling Center (M-F 8 a.m. to 5 p.m. at 405-325-2911).

Because the University of Oklahoma is committed to the safety of you and other students, and because of our Title IX obligations, I, as well as other faculty, Graduate Assistants, and Teaching Assistants, are mandatory reporters. This means that we are obligated to report gender-based violence that has been disclosed to us to the Institutional Equity Office. This means that we are obligated to report gender-based violence that has been disclosed to us to the Institutional Equity Office. This includes disclosures that occur in: class discussion, writing assignments, discussion boards, emails and during Student/Office Hours. You may also choose to report directly to the Institutional Equity Office. After a report is filed, the Title IX Coordinator will reach out to provide resources, support, and information and the reported information will remain private. For more information regarding the University's Title IX Grievance procedures, reporting, or support measures, please visit Institutional Equity Office at 405-325-3546.

Reasonable Accommodation Policy

The University of Oklahoma (OU) is committed to the goal of achieving equal educational opportunity and full educational participation for students with disabilities. If you have already established reasonable accommodations with the Accessibility and Disability Resource Center (ADRC), please submit your semester accommodation request through the ADRC as soon as possible and contact me privately, so that we have adequate time to arrange your approved academic accommodations.

If you have not yet established services through ADRC, but have a documented disability and require accommodations, please complete ADRC's pre-registration form to begin the registration process. ADRC facilitates the interactive process that establishes reasonable accommodations for students at OU. For more information on ADRC registration procedures, please review their Register with the ADRC web page. You may also contact them at (405)325-3852 or adrc@ou.edu, or visit www.ou.edu/adrc for more information.

Note: disabilities may include, but are not limited to, mental health, chronic health, physical, vision, hearing, learning and attention disabilities, pregnancy-related. ADRC can also support students experiencing temporary medical conditions.

Religious Observance

It is the policy of the University to excuse the absences of students that result from religious observances and to reschedule examinations and additional required classwork that may fall on religious holidays, without penalty. [See Faculty Handbook 3.15.2]

Adjustments for Pregnancy/Childbirth Related Issues

Should you need modifications or adjustments to your course requirements because of documented pregnancy-related or childbirth-related issues, please contact the Accessibility and Disability Resource Center at 405/325-3852 and/or the Institutional Equity Office at 405/325-3546 as soon as possible. Also, see the Institutional Equity Office FAQ on Pregnant and Parenting Students' Rights for answers to commonly asked questions.

Final Exam Preparation Period

Pre-finals week will be defined as the seven calendar days before the first day of finals. Faculty may cover new course material throughout this week. For specific provisions of the policy please refer to OU's Final Exam Preparation Period policy.

Emergency Protocol

During an emergency, there are official university procedures that will maximize your safety.

Severe Weather: If you receive an OU Alert to seek refuge or hear a tornado siren that signals severe weather.

1. Look for severe weather refuge location maps located inside most OU buildings near the entrances.
2. Seek refuge inside a building. Do not leave one building to seek shelter in another building that you deem safer. If outside, get into the nearest building.
3. Go to the building's severe weather refuge location. If you do not know where that is, go to the lowest level possible and seek refuge in an innermost room. Avoid outside doors and windows.
4. Get in, Get Down, Cover Up
5. Wait for official notice to resume normal activities.

Additional Weather Safety Information is available through the Department of Campus Safety.

The University of Oklahoma Active Threat Guidance

The University of Oklahoma embraces a Run, Hide, Fight strategy for active threats on campus. This strategy is well known, widely accepted, and proven to save lives. To receive emergency campus alerts, be sure to update your contact information and preferences in the account settings section at one.ou.edu.

RUN: Running away from the threat is usually the best option. If it is safe to run, run as far away from the threat as possible. Call 911 when you are in a safe location and let them know from which OU campus you're calling from and location of active threat.

HIDE: If running is not practical, the next best option is to hide. Lock and barricade all doors; turn of all lights; turn down your phone's volume; search for improvised weapons; hide behind solid objects and walls; and hide yourself completely and stay quiet. Remain in place until law enforcement arrives. Be patient and remain hidden.

FIGHT: If you are unable to run or hide, the last best option is to fight. Have one or more improvised weapons with you and be prepared to attack. Attack them when they are least expecting it and hit them where it hurts most: the face (specifically eyes, nose, and ears), the throat, the diaphragm (solar plexus), and the groin.

Please save OUPD's contact information in your phone.

NORMAN campus: *For non-emergencies call (405) 325-1717. For emergencies call (405) 325-1911 or dial 911.*

TULSA campus: *For non-emergencies call (918) 660-3900. For emergencies call (918) 660-3333 or dial 911.*

Fire Alarm/General Emergency

If you receive an OU Alert that there is danger inside or near the building, or the fire alarm inside the building activates:

1. *LEAVE* the building. Do not use the elevators.
2. *KNOW* at least two building exits
3. *ASSIST* those that may need help
4. *PROCEED* to the emergency assembly area
5. *ONCE safely outside, NOTIFY first responders of anyone that may still be inside building due to mobility issues.*
6. *WAIT* for official notice before attempting to re-enter the building.

OU Fire Safety on Campus